REMARKS

The Office Action dated August 2, 2007 has been received and considered. In this response, claims 1, 9, and 16 have been amended. Claims 19 and 20 have been added. Support for the amendments and new claims may be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 1-3, 7 and 16

At page 2 of the Office Action, claims 1-3, 7 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baird (U.S. Patent No. 6,204,787 B1) in view of Nonoyama et al. (U.S. Patent No. 6,529,025). This rejection is hereby respectfully traversed.

Claim 1 as amended recites "a second set of switches…configured to transfer the first charge and a second charge to the integrator input **during a second phase**, the second charge proportional to the DC offset component and **based on a voltage applied in series with the pair of capacitors during the second phase**." The Office Action at page 3 acknowledges that Baird fails to disclose or suggest these elements, and turns to Nonoyama. Nonoyama discloses a capacitor 51 with one terminal connected to a ground reference and another terminal connected to a switch 52 and a switch 53. *Nonoyama*, FIG. 1. During a first phase, labeled "c", the switch 52 transfers a charge based on an offset voltage to the capacitor 51. *Id.*, FIG. 1, FIG. 2, col. 6, lines 42-53. During a second phase, labeled "a", the switch 53 transfers the charge stored at the capacitor 51 to an integrator 6. *Id.* Accordingly, Nonoyama discloses that the application of the offset voltage to a capacitor and the transfer of the capacitor charge to an integrator **occur in two separate phases**. In contrast, claim 1 as amended recites that the second set of switches is configured to transfer charge from a pair of capacitors during **the same phase in which an offset voltage is applied to the capacitor pair**. Accordingly, the cited references, individually and in combination, fail to disclose at least one element of claim 1.

Claims 2-3 depend from claim 1. Accordingly, the cited references fail to disclose each and every element of these dependent claims, at least by virtue of their dependency on claim 1. In addition, claims 2 and 3 recite additional novel elements.

Claim 7 recites "a second set of switches…configured to transfer the first charge and a second charge to the integrator input during **a second phase**, the second charge proportional to the DC offset component and **based on a voltage applied in series with the pair of capacitors during the second phase**." As explained above, the cited references fail to disclose or suggest these elements.

With respect to claim 16, the claim recites "**during a second phase**, applying a voltage in series with the pair of capacitors to provide a DC offset correction charge" and "**during the second phase**, transferring a sum charge via the pair of capacitors to inputs of a first integrator…the sum charge including the reference charge and the DC offset correction charge." At page 5, the Office Action relies on Nonoyama as disclosing transferring a sum charge via a pair of capacitors where the sum charge includes a reference charge and a DC offset correction charge. However, Nonoyama does not disclose applying a voltage in series with a pair of capacitors to provide the DC offset correction charge **during the same phase** as the sum charge is transferred to an integrator. Further, Baird does not remedy the deficiency of Nonoyama. Accordingly, the cited references, individually and in combination, fail to disclose or suggest at least one element of claim 16.

In view of the forgoing, it is respectfully submitted that the obviousness rejection of claims 1-3, 7 and 16 is improper. Withdrawal of this rejection and reconsideration of the claims therefore is respectfully requested.

Obviousness Rejection of Claims 4-6, 8, 17 and 18

At page 5 of the Office Action, claims 4-6, 8, 17 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baird and Nonoyama et al., as applied to claim 1 above, and further in view of Ferguson, Jr. et al. (U.S. Patent No. 6,040,793). This rejection is hereby respectfully traversed.

Claims 4-6 depend from claim 1. Claim 8 depends from claim 7. Claim 17 and 18 depend from claim 16. As explained above, Baird and Nonoyama fail to disclose or suggest at least one element of each of claims 1, 7 and 16. Further, Ferguson does not remedy the deficiencies of the other cited references. Accordingly, the cited references fail to disclose each

and every element of the dependent claims, at least by virtue of their respective dependency on claims 1, 7, and 16. In addition, claims 4-6, 8, 17, and 18 recite additional novel elements.

To illustrate, claim 4 recites "a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output, wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal." The Office Action at pages 5-6 acknowledges that the fourth set of switches is not disclosed by Baird and Nonoyama, and turns to Ferguson. Ferguson discloses a set of switches to change polarity of a feedback voltage. *Ferguson*, FIG. 2. However, Ferguson does not disclose or suggest that the polarity of the feedback voltage is related to a DC offset component in any manner, and accordingly fails to disclose or suggest "the polarity of the second charge is configured to cancel the DC offset component of the input signal" as recited in claim 4.

With respect to claim 5, the claim recites "a digital to analog converter coupled to the pair of capacitors for producing the second charge." The Office Action at page 6 relies on Ferguson as disclosing these elements. Ferguson discloses a one-bit digital to analog converter (DAC) in a feedback path. *Id.*, col. 1, lines 63-64. Based on a digital input, the DAC of Ferguson provides a positive or negative reference voltage. *Id.*, col. 1, line 64 –col. 2, line 2. Accordingly, the DAC of Ferguson provides a **reference voltage**. However, the DAC recited in claim 5 provides the second charge, which as recited in claim 1 **is proportional to a DC offset**. There is no disclosure that the reference voltage provided by the Ferguson DAC is related to a DC offset in any manner. Accordingly, the cited references fail to disclose or suggest at least one element of claim 5.

In view of the forgoing, it is respectfully submitted that the obviousness rejection of claims 4-6, 8, 17 and 18 is improper. Withdrawal of this rejection and reconsideration of the claims therefore is respectfully requested.

Obviousness Rejection of Claims 9 and 10

At page 7 of the Office Action, claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baird in view of Nonoyama et al., and further in view of Bazarjani et al. (U.S. Patent No. 6,005,506). This rejection is hereby respectfully traversed.

Claims 9 and 10 depend from claim 7. As explained above, Baird and Nonoyama fail to disclose or suggest at least one element of each of claim 7. Further, Bazarjani does not remedy the deficiencies of the other cited references. Accordingly, the cited references fail to disclose each and every element of the dependent claims, at least by virtue of their dependency on claim 7. In addition, claims 9 and 10 recite additional novel elements.

In view of the forgoing, it is respectfully submitted that the obviousness rejection of claims 9 and 10 is improper. Withdrawal of this rejection and reconsideration of the claims therefore is respectfully requested.

Obviousness Rejection of Claims 11-15

At page 9 of the Office Action, claims 11-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baird, Nonoyama et al. and Bazarjani et al., as applied to claim 9 above, and further in view of Ferguson, Jr. et al. This rejection is hereby respectfully traversed.

Claims 11-15 depend from claim 7. As explained above, Baird and Nonoyama fail to disclose or suggest at least one element of each of claim 7. Further, Bazarjani does not remedy the deficiencies of the other cited references. Accordingly, the cited references fail to disclose each and every element of the dependent claims, at least by virtue of their dependency on claim 7. In addition, claims 11-15 recite additional novel elements

In view of the forgoing, it is respectfully submitted that the obviousness rejection of claims 11-15 is improper. Withdrawal of this rejection and reconsideration of the claims therefore is respectfully requested.

Obviousness Rejection of Claims 1 and 16

At page 12 of the Office Action, claims 1 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ferguson, Jr. et al. in view of Nonoyama et al. This rejection is hereby respectfully traversed.

Claim 1 recites "a second set of switches…configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase." The Office Action at page 12 acknowledges that Ferguson fails to

disclose or suggest these elements, and turns to Nonoyama. However, as explained above, Nonoyama also fails to disclose or suggest these elements. Accordingly, the cited references fail to disclose or suggest at least one element of claim 1.

With respect to claim 16, the claim recites "during a second phase, applying a voltage in series with the pair of capacitors to provide a DC offset correction charge" and "during the second phase, transferring a sum charge via the pair of capacitors to inputs of a first integrator…the sum charge including the reference charge and the DC offset correction charge." As explained above, Nonoyama fails to disclose these elements. Further, Ferguson does not remedy the deficiencies of Nonoyama. Accordingly, the cited references fail to disclose or suggest at least one element of claim 16.

In view of the forgoing, it is respectfully submitted that the obviousness rejection of claims 1 and 16 is improper. Withdrawal of this rejection and reconsideration of the claims therefore is respectfully requested.

New Claims 19 and 20

Claims 19 and 20 have been added. The cited references fail to disclose or suggest at least one element of each of claims 19 and 20. Accordingly, consideration and allowance of claims 19 and 20 is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

It is believed no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-3797.

Respectfully submitted,

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Date